Tutorials

T1: Introduction to Fractional-*N* Phase-Locked Loops

This tutorial begins with a brief review of integer-*N* PLLs, and then, presents a detailed explanation of the additional ideas and issues associated with the extension to fractional-*N* PLLs for frequency synthesis. Topics include a self-contained explanation of the relevant aspects of $\Delta\Sigma$ modulation, an extension of the well-known integer-*N* PLL linearized model to fractional-*N* PLLs, the non-ideal effects of particular concern in fractional-*N* PLLs such as charge-pump nonlinearities and data-dependent divider delays, and techniques for wideband in-loop digital modulation of the VCO. Case studies of example circuits and applications are presented to illustrate the main concepts.

Instructor: **Ian Galton** received his Sc.B. from Brown University, in 1984, and his M.S. and Ph.D. from the California Institute of Technology, in 1989 and 1992, respectively, all in electrical engineering. Since 1996, he has been a professor of electrical engineering at the University of California, San Diego, where he teaches and conducts research in the field of mixed-signal integrated circuits and systems for communications. Prior to 1996, he was with UC Irvine, the NASA Jet Propulsion Laboratory, Acuson, and Mead Data Central. His research involves the invention, analysis, and integrated-circuit implementation of critical communication-system building blocks, such as data converters, frequency synthesizers, and clock- recovery systems. In addition to his academic research, he regularly consults at several semiconductor companies, and teaches industry-oriented short courses on the design of mixed-signal integrated circuits. He has served as a member of a corporate Board of Directors, as a member of several corporate Technical Advisory Boards, and as the Editor-in-Chief of the IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing.

T2: Data-Converter Interfaces: The Analog and Digital Ins and Outs

Many of the critical performance characteristics of Data Converters are determined by their input and output circuitry. This tutorial will provide a high-level overview of how different architectural and circuit choices impact the analog, digital, reference, and clock interfaces, in today's A/D and D/A converter designs, and how this ultimately may limit the converter's performance under different application conditions.

Instructor: David Robertson is a Product-Line Director of the High-Speed-Converter Group at Analog Devices. He received his B.A. and B.E. degrees from Dartmouth College, in 1984 and 1985, respectively, and since 1985 has worked at Analog Devices on a wide variety of D/A and A/D converters on complementary bipolar, BiCMOS, and CMOS processes. Dave currently holds 14 patents on converter and mixed-signal circuits, has participated in two "outstanding-panel" ISSCC evening panel sessions, and was co-author of the paper that received the IEEE Journal of Solid-State Circuits 1997 Best Paper Award.

T3: Introduction to Statistical Variation and Techniques for Design Optimization

Variability is a reality in nanometer semiconductor processes. This tutorial will cover the sources of systematic and random variations of transistors and their surrounding interconnects. Included in the variability discussion will be within-chip variability, across-wafer variability, across-device variability, and device mismatch. The resulting impact upon an individual circuit's functionality and timing will be explored. Analytical approaches will be shown for examining the variability's impact upon leakage power, dynamic power, and circuit functionality of static and dynamic circuits, SRAM arrays, and PLLs. Techniques will include Monte-Carlo analysis, vector analysis, and statistical timing analysis.

Instructor: Norman Rohrer is a Distinguished Engineer in the PowerPC-Microprocessor Group within the System-and-Technology Group of IBM, located in Essex Junction, VT. Norman received his Bachelor's Degree in physics and mathematics from Manchester College, North Manchester, IN, in 1987. He received his Master's Degree and Doctor of Philosophy degree in electrical engineering from Ohio State University, Columbus, OH, in 1990 and 1992, respectively. Norman has been a lead designer on PowerPC 750 and 970 products for Apple's G3 and G5 chips, and Nintendo's GameCube. His interests lie in the area of high-speed circuit optimization for future technologies. Norman holds 18 patents, and is a co-author of two books titled "*High-Speed CMOS Circuit-Design Styles",* and "*SOI Circuit-Design Concepts".*

T4: Introduction to CMOS Bio-Sensors: Electrical Specifications, CMOS Processing, Circuit and System Design

Silicon-based bio-sensors and bactuators have attracted much attention for a number of years — particularly if equipped with on-chip intelligence, i.e., CMOS circuitry. On the other hand, although there are a number of promising developments in this area, most of them focus, so far, on niche applications, but, commercialization of a number of approaches is still ongoing. It is thus sometimes difficult to distinguish whether a CMOS chip in this area is a "Me-too" demonstrator, competitive to other non-electronic technologies, or indeed provides a unique selling-point worthy of further development.

This talk will present an overview of the current status of CMOS approaches for in-vitro applications in life sciences and biotechnology, such as drug screening and medical diagnosis. Starting with a review of the operating principles and applications of the related sensors and actuators, required CMOS-processing extensions are considered, electrical specifications and related circuit requirements are derived, concrete circuit designs purpose are presented, and advantages and drawbacks compared to existing non-CMOS-based techniques (if available) are discussed. Chips and data presented in the literature considered to provide examples illustrating the above-mentioned issues.

Instructor: Roland Thewes received his Dipl.-Ing. and Dr.-Ing. in Electrical Engineering from the University of Dortmund, Germany, in 1990 and 1995, respectively. Since 1994, he has been with the Research Laboratories of Siemens and Infineon, where he was active in the design of non-volatile memories and in the field of reliability and yield of analog CMOS circuits. From 1997 to 1999, he managed projects in the fields of design-for-manufacturability, reliability, analog-device performance, and analog-circuit design. Since 2000, he has been responsible for the Laboratory on Mixed-Signal Circuits in Corporate Research of Infineon Technologies, and for the development of CMOS-based biosensors. He lectures at the University of Ulm, and serves as a member of the technical program committees of ESSDERC, IEDM, and ISSCC.

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T5: Multi-Level Cell Design for Flash Memory

Flash Memory with multi-level cells was first reported at ISSCC in 1995. Since then, it has become commercially available in high volume from many semiconductor manufacturers. Multi-level design achieves the storage of more than two analog levels in a flash memory cell. If four analog levels are stored in a single flash cell, two bits of information can be programmed into the cell. This essentially reduces the cell area by half relative to single-bit storage, and can approach the same cost savings (from a memory-array perspective) as a change in one lithography generation. This tutorial explores some of the basic Multi-Level-Cell design techniques for Flash Memory, and will include:

- Basic concepts of multi-level analog storage relative to single-bit-per-cell storage
- The need for precise charge placement and precise charge sensing of floating-gate memory cells
- Circuit design and chip-architectural techniques to achieve multi-level analog storage of more than one bit per cell

Instructor: Mark Bauer is currently Senior Principal Engineer at Intel Corporation in Folsom, California, where he is responsible for advanced circuit design and Flash-memory technology development. He received his BSEE in Electrical Engineering in 1985 from the University of California at Davis. Upon graduation, Mark joined Intel's Memory Components Division, working on EPROM design. He started working on Flash-memory design in 1992, and was responsible for circuit-design and technology development for the first Intel StrataFlash™ memory. He has served on the ISSCC memory sub-committee since 1999. He has authored several technical papers, one of which won the Lewis Winner Award for Outstanding Paper at ISSCC (1995). He holds more than 20 patents in the field of Non-Volatile Memory.

T6: Cellular-Phone Applications Trends and DSP Technology

As the cellular phone spreads worldwide, its applications are rapidly expanding and becoming more and more attractive. These applications are based on digital-signal processing, for which high performance with low power consumption is required. From performance, cost, and power-consumption points of view, this tutorial will focus on multimedia applications and the related DSP technologies needed on the cellular phone, including;

Multimedia applications – Video- and audio-processing algorithms – Multimedia DSP architectures – Low-power circuit designs

Instructor: Masafumi Takahashi is currently a Chief Specialist at Toshiba Corporation Semiconductor in Kawasaki, Japan, where he is involved in the development of multimedia SoCs for mobile applications, focusing on audio-visual processing architectures and low-power circuit techniques. He joined Toshiba Corporation in 1987, where he was engaged in research on multiprocessor architectures until 1996. He has been a member of the ISSCC Signal Processing Sub-Committee since 2004. He received his ME from the University of Tsukuba, Japan in 1987.

T7: 3D Integration

Limitations to continued CMOS scaling are motivating interest in technologies which improve performance by reducing latency and increasing bandwidth. Such a development is in 3D chip technologies which come in many flavors and styles, but are receiving lots of attention lately, as a means of extending power-performance in high-end systems. Designing for three dimensions, however, forces us to look at formerly-two-dimensional integration issues, quite differently. A number of commercial offerings and research programs suggest ways of addressing these challenges. This tutorial will survey present development directions in 3D, and introduce some of the opportunities this exciting new technology creates.

Instructor: Kerry Bernstein is a Senior Technical Staff Member at the IBM T.J. Watson Research Center, Yorktown Hts, NY. He is currently responsible for future-product-technology definition, performance, and application. Kerry received his B.S in electrical engineering from Washington University in St.Louis, and joined IBM in 1978. He holds 50 US Patents, and is a co-author of 3 college textbooks and multiple papers on high-speed and low-power CMOS. His interests are in the area of high-performance low-power advanced circuit technologies. He is a staff instructor at RUNN/Marine Biological Laboratories, Woods Hole, MA.

T8: Millimeter-Wave ICs in Silicon

There is a plethora of emerging applications at high-microwave and millimeter-wave frequencies (e.g., at 24GHz, 60GHz, and 77GHz) that offer new opportunities and challenges for silicon implementation. This tutorial covers circuit design for some of these emerging applications, such as gigabit wireless Ethernet (GWE), and automotive radar. We will discuss some of the primary issues for integrated millimeter-wave circuits, and some of the circuit and system techniques that can be applied at such high frequencies, with a focus on distributed circuits and multiple-antenna-array approaches, and their resulting system improvements.

Instructor: Ali Hajimiri received his B.S. in electronics engineering from the Sharif University of Technology, and his M.S. and Ph.D. in electrical engineering from Stanford University, Stanford, CA. He has been with Philips Semiconductors, Sun Microsystems, and Lucent Technologies (Bell Labs) in Murray Hill. In 1998, he joined the faculty of the California Institute of Technology, Pasadena, where he is an Associate Professor of Electrical Engineering, and the director of the Microelectronics Laboratory. Ali holds several U.S. and European patents. He is an Associate Editor of the JSSC, and a member of the Technical Program Committee of the ISSCC. Ali was selected as one of the top-100 innovators (TR100) in 2004.

T9: Signal Integrity for High-Speed Circuit Designers

Signal integrity issues will be explained for beginning high-speed circuit designers. This tutorial will cover the operation principles of transmission lines on FR4 PCB, SPICE parameters for passive elements, signaling methods, compensation methods for channel loss, SPICE simulation examples using IBIS models, and power-integrity issues.

Instructor: Hong-June Park is a Professor at the POSTECH (Pohang University of Science and Technology) in Pohang, Korea. He is involved in the design of high-speed CMOS interface circuits and the signal-integrity issues associated with 2 to 5Gb/s DRAM interfaces. He received his PhD in Electrical Engineering from the University of California at Berkeley, in 1989.